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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/007,300	11/08/2001	Keiji Jono	KM1-003	4689

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EXAMINER
TRAN, THIEN F

ART UNIT	PAPER NUMBER
2811	5

DATE MAILED: 01/29/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/007,300	Applicant(s) JONO ET AL.	
	Examiner Thien F Tran	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 33-69 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 33-69 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

The abstract of the disclosure is objected to because the invention is about the device, not the process of making the device. Therefore, the abstract should be directed to the device, its structure and operation instead of the steps of forming the device. Correction is required. See MPEP § 608.01(b).

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed, the invention is about a device not a method of making the device.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 42-46 are rejected under 35 U.S.C. 102(a) as being anticipated by Sakai et al. (USPN 6,034,409)

Sakai et al. discloses the claimed trench isolation structure (Fig. 7) formed in a semiconductor 1 comprising a first isolation trench portion 11a having a first depth and having a first sidewall intersecting a surface of the semiconductor at a first angle A1; a second isolation trench portion 11 within and extending below the first isolation trench portion, the second isolation trench portion having a second depth and including a second sidewall intersecting the first sidewall at a second angle A2 with respect to the

surface that is greater than the first angle; and a dielectric material 4 filling the first and second isolation trench portions.

Regarding claim 43, at least some of the first isolation trench portion forms a substantially straight linear segment.

Regarding claims 44 and 45, the first angle A1 and the second angle A2 are within the claimed range.

Regarding claim 46, the first depth is between five and fifty percent of a total trench depth.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 47 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakai et al. (USPN 6,034,409).

Sakai et al. as described above does not disclose the trench isolation structure being formed in a memory integrated circuit. It is well known in the art that a memory integrated circuit comprising memory transistors and trench isolation structure for isolating transistors from each other. It would have been obvious to form the trench isolation structure as taught by Sakai et al. as a part of the conventional memory integrated circuit to ensure required device isolation characteristics and to obtain good electrical characteristics.

Claims 33-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noguchi (USPN 5,969,393) in view of Sakai et al. (USPN 6,034,409).

Noguchi discloses a trench isolated transistor (Figs. 2A-2B) comprising first and second isolation trenches each disposed on a respective side of a portion of silicon 101, a gate 108 extending across the silicon portion from the first isolation trench to the second isolation trench; and source and drain regions 109 extending between the first and second isolation trenches and across the silicon portion, the source region being disposed adjacent one side of the gate and the drain region being disposed adjacent another side of the gate that is opposed to the one side. Noguchi does not disclose the first and second isolation trenches each comprising a first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the silicon at a first angle; a second isolation trench portion within and extending below the first isolation trench portion, the second isolation trench portion having a second depth and including a second sidewall intersecting the first sidewall at a second angle with respect to the surface that is greater than the first angle; and a dielectric material filling the first and second isolation trench portions. Sakai et al. as described above discloses a trench isolation structure comprising a first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the silicon at a first angle; a second isolation trench portion within and extending below the first isolation trench portion, the second isolation trench portion having a second depth and including a second sidewall intersecting the first sidewall at a second angle with respect to the surface that is greater than the first angle; and a dielectric material filling the first and second isolation

trench portions. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the first and second isolation trenches of Noguchi using the trench isolation structure as taught by Sakai et al. so that the first and second isolation trenches each comprises a first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the silicon at a first angle; a second isolation trench portion within and extending below the first isolation trench portion, the second isolation trench portion having a second depth and including a second sidewall intersecting the first sidewall at a second angle with respect to the surface that is greater than the first angle; and a dielectric material filling the first and second isolation trench portions in order to ensure sufficient device isolation characteristics and obtain good electrical characteristics.

Regarding claim 34, at least some of the first sidewall forms a substantially straight linear segment.

Regarding claims 35, 36, 39 and 40, the first angle A1 and the second angle A2 are within the claimed range.

Regarding claim 37, the first depth is between five and fifty percent of a total trench depth.

Regarding claim 38, the dielectric material filling the first and second isolation trench portions has a planar surface.

Regarding claim 41, the modified Noguchi does not disclose the trench-isolated transistor being formed as a part of a memory integrated circuit. However, it is well known in the art that a conventional memory integrated circuit comprising memory

transistors and trench isolation structure for isolating transistors from each other. It would have been obvious to form the trench isolated transistor structure as taught by Noguchi and Sakai et al. as a part of the conventional memory integrated circuit to ensure required device isolation characteristics and to obtain good electrical characteristics.

Claims 48-54 and 62-69 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noguchi (USPN 5,969,393) and Sakai et al. (USPN 6,034,409) as applied to claims 33-41 above, and further in view of Wang et al. (USPN 6,171,924).

The combined Noguchi and Sakai et al. references as described above disclose a trench-isolated transistor but do not disclose the trench isolated transistor being formed as a part of a DRAM memory cell that comprises a transistor and a storage capacitor. However, a DRAM memory cell is well known structure in the semiconductor device as shown for example by Wang et al. Wang et al. discloses a memory cell (Fig. 1) including a capacitor; a transistor having a gate, a drain and a source, the source being coupled to one terminal of the capacitor; a bitline coupled to the drain, and a wordline coupled to the gate. Therefore, it would have been obvious to form the trench isolated transistor structure as taught by Noguchi and Sakai et al. as a part of the memory cell of Wang et al. in order to ensure required device isolation characteristics and to obtain good electrical characteristics.

Regarding claims 49 and 63, Noguchi discloses the gate comprises polysilicon.

Regarding claims 50 and 64, at least some of the first sidewall forms a substantially straight linear segment.

Regarding claims 51, 52, 65 and 66, the first angle A1 and the second angle A2 are within the claimed range.

Regarding claims 53 and 67, the first depth is between five and fifty percent of a total trench depth.

Regarding claims 54 and 68, the memory cell is included within a DRAM integrated circuit.

Regarding claim 69, the second isolation trench comprises a third isolation trench portion having the first depth and having a third sidewall intersecting the surface at the first angle; a fourth isolation trench portion within and extending below the third isolation trench portion, the fourth isolation trench portion having the second depth and including a fourth sidewall intersecting the third sidewall at the second angle.

Claims 55-61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noguchi (USPN 5,969,393) and Sakai et al. (USPN 6,034,409) and Wang et al. (USPN 6,171,924) as applied to claims 48-54 above, and further in view of Kim (USPN 6,154,417).

The combined Noguchi, Sakai et al. and Wang et al. references as described above disclose a DRAM memory device but do not specifically disclose the DRAM memory device further comprising address decoding circuitry, a group of bitlines coupled to the address decoding circuitry and extending in a first direction; a group of wordlines coupled to the address decoding circuitry and extending in a second direction, each wordline in the group of wordlines intersecting each of the bitlines in the group of bitlines once at an intersection. However, a DRAM memory device comprising address

decoding circuitry, a group of bitlines coupled to the address decoding circuitry and extending in a first direction; a group of wordlines coupled to the address decoding circuitry and extending in a second direction, each wordline in the group of wordlines intersecting each of the bitlines in the group of bitlines once at an intersection is widely used and known in the art as shown for example by Kim (see Fig. 1). Therefore, forming the DRAM device comprising conventional elements like address decoding circuitry, a group of bitlines coupled to the address decoding circuitry and extending in a first direction; a group of wordlines coupled to the address decoding circuitry and extending in a second direction, each wordline in the group of wordlines intersecting each of the bitlines in the group of bitlines once at an intersection would have been obvious modification in order to read, write data to all memory cells in the memory array more efficiently.

Regarding claim 57, Noguchi discloses the gate comprises polysilicon.

Regarding claim 56, at least some of the first sidewall forms a substantially straight linear segment.

Regarding claims 58 and 59, the first angle A1 and the second angle A2 are within the claimed range.

Regarding claim 60, the first depth is between five and fifty percent of a total trench depth.

Regarding claim 61, the dielectric material filling the first and second isolation trench portions includes a planar outer surface.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thien F Tran whose telephone number is (703) 308-4108. The examiner can normally be reached on 8:30AM - 5:00PM Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

tt
January 24, 2003

Thien Tran
Patent Examiner
Technology Center 2800